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EXAMINER	
BOWMAN, MARY ELLEN	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/594,904	SAKEMURA ET AL.	
	Examiner	Art Unit	
	MARY ELLEN BOWMAN	4174	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06 December 2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 06 December 2006 was considered by the examiner.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims **1-13 and 15** are rejected under 35 U.S.C. 102(b) as being anticipated by Brune et al., WO 02/05305 A1, published January 17, 2002 (hereinafter referred to as "Brune"). Note: Brune was cited by Applicant and is therefore not included in the attached Notice of References Cited.

5. Regarding claim 1, Brune teaches an electron emitting device having a lower electrode near a substrate and an upper electrode far from the substrate respectively (e.g., p. 7, par. 1; "an electron emitting device comprises parallel spaced-apart first conductors 10 [i.e., lower electrode] intersecting with parallel spaced-apart second conductors 11 [i.e., upper electrode]"), formed of a plurality of electron emitting elements which emit electrons from a side of the upper electrode (e.g., p. 7, par. 1; "at their intersections [i.e., intersection of lower and upper

electrode]…where electrons 12 are emitted…electrons that travel ballistically through and are emitted at 12 from the second conductors 11 [i.e., through the upper electrode]"), characterized in that the electron emitting elements are made independent and in that space is formed therebetween (e.g., Figure 2 below; electron emitting elements 12 are independent and spaced apart), and in that the upper electrode extends across the plurality of electron emitting elements and the space by a bridging portion of the upper electrode (e.g., Figure 2 below; upper electrode 11 extends across the space between the electron emitting elements 12).

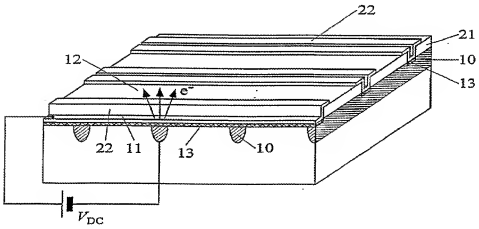


Fig. 2

6. Regarding claim 2, Brune teaches the invention as explained above regarding claim 1 and further teaches the bridge portion is provided with at least one through hole or notched portion (e.g., Figure 2 above, upper electrode 11 is provided with a notched portion corresponding to the bridge portion of the electrode that extends over electron emitting elements 12 as explained above regarding claim 1).

7. Regarding claim 3, Brune teaches the invention as explained above regarding claim 2 and further teaches the through hole or notched portion is circular-shaped, rectangular-shaped,

diamond-shaped, barrel-shaped, star-shaped, shoulder drum shaped, or a shape formed of part of these shapes (e.g., Figure 2 above, the notched portion of upper electrode 11 is rectangular shaped).

8. Regarding claim 4, Brune teaches the invention as explained above regarding claim 1 and further teaches the bridge portion extends approximately parallel to the substrate (e.g., Figure 2 above, the bridge portion of the upper electrode 11 which extends over electron emitting elements 12 is approximately parallel to the substrate).

9. Regarding claim 5, Brune teaches the invention as explained above regarding claim 1 and further teaches both the lower electrode, and the upper electrode connected at the bridge portions or strip shaped electrodes arranged in positions that are mutually orthogonal (e.g., Figure 2 above, stripe shaped lower electrode 10 and stripe shaped upper electrode 11 intersect at the bridge portions and are mutually orthogonal).

10. Regarding claim 6, Brune teaches the invention as explained above regarding claim 1 and further teaches the upper electrode extends over a plurality of electron emitting elements and spaces by the bridge portions without the electron emitting elements being limited to the row or column directions (e.g., p. 7, par. 1; "at their intersections addressable locations where electrons 12 are emitted"; Note: The intersections of lower and upper electrodes 10 and 11 occur in both row and column directions, and therefore the electron emitting elements are not limited to either row or column directions), and the lower electrode is separated and independent for each electron emitting element (e.g., Figure 2 above, lower electrode 10 is formed in separated stripes and is therefore separate and independent for each electron emitting element).

11. Regarding claim 7, Brune teaches the inventions as explained above regarding claim 5 or 6 and further teaches the electron emitting elements further comprise and insulator layer and an electron supply layer made from a semiconductor deposited between the lower electrode and the upper electrode (e.g., p. 7, par. 4; "the device can also be produced using mainstream C-MOS technology"; Note: MOS is a well known acronym for metal-oxide-semiconductor, indicating the electron emitting element comprises a semiconductor layer between the two electrodes), and when a voltage is applied between the lower electrode an the upper electrode electrons are emitted from the upper electrode (e.g., p. 7, par. 1; "hot electrons...are emitted at 12 from the second conductors 11 in response to the application of the energizing voltage V").

12. Regarding claim 8, Brune teaches the invention as explained above regarding claim 7 and further teaches the bridge portion comprises the material of the insulator layer that is integral with the insulator layer of the electron emitting element (e.g., p. 8, pars. 1 and 2; "on top of the wafer 20 [i.e., substrate] is then grown a film 21 of thermal SiO_2...structured to yield a pattern of parallel strips [i.e., bridging portion]...the wafer is 20 is then overgrown with a...thermal oxide 21 yielding stripes 13 [i.e., the insulator layer of the electron emitting element]").

13. Regarding claim 9, Brune teaches the invention as explained above regarding claim 1 and further teaches the electron supply layer is made from an amorphous phase that comprises silicon or a mixture or compound whose main component is silicon (e.g., p. 7, par. 4; "a Si (1001) wafer 20 is heavily doped in a stripe pattern...on top of the wafer 20 is then grown a film 21 of thermal SiO_2...this oxide film 21 is then structured to yield a pattern of parallel stripes").

14. Regarding claim 10, Brune teaches the invention as explained above regarding claim 1 and further teaches at least one electron emitting section formed from an island area in which the

film thickness of the insulator layer and the upper electrode gradually decreases towards the electron supply layer (e.g., Figure 2 below, the thickness of the insulator layer 21 and upper electrode layer 11 steps down, or gradually decreases, to form island areas over each electron emitting element).

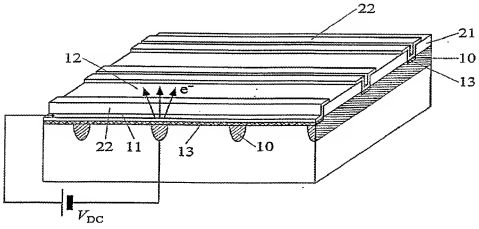


Fig. 2

15. Regarding claim 11, Brune teaches the invention as explained above regarding claim 10 and further teaches in the island areas the upper electrode terminates on the insulator layer (e.g., Figure 2 above, upper electrode 11 terminates as metal layer 22 on insulator layer 21).

16. Regarding claim 12, Brune teaches the inventions as explained above regarding claim 10 or 11 and further teaches in the island areas the insulator layer terminates on the electron supply layer (e.g., Figure 2 above, insulator layer 21 terminates on electron supply layer 13 at the island areas).

17. Regarding claim 13, Brune teaches the invention as explained above regarding claim 10 and further teaches the island areas are depressions in the flat surface of the upper electrode (e.g., Figure 2 above, island areas are depressions in the flat surface of upper electrode 11).

18. Regarding claim 15, Brune teaches the invention as explained above regarding claim 10 and further teaches electrically insulating masks are provided in the island areas (e.g., p. 8, par. 2; "depositing photoresist [i.e., electrically insulating masks] on the thick oxide areas 21 in-between the stripes 13").

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claim **14** is rejected under 35 U.S.C. 103(a) as being unpatentable over Brune.

21. Brune teaches the invention as explained above regarding claim 10, and further teaches the insulator layer is made from dielectric material, and a part other than the island areas has a film thickness of 50 nm or greater (e.g., p. 8, par. 1; "a film 21 of thermal SiO_2 [i.e., a dielectric] having a thickness of 20 nm or more [i.e., a range including the claimed 50 nm or greater]").

22. It would have been obvious to one of ordinary skill in the art at the time the invention was made to optimize the range of 20 nm or more insulation thickness as taught by Brune, to 50 nm or more insulation thickness as claimed, because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

23. Claims **16 and 24-27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Brune in view of Kikuchi et al., USPN 6,297,587 B1, published October 2, 2001 (hereinafter referred to as "Kikuchi").

24. Regarding claim 16, Brune teaches the invention as explained above regarding claim 10, but fails to teach a carbon electron emitter.

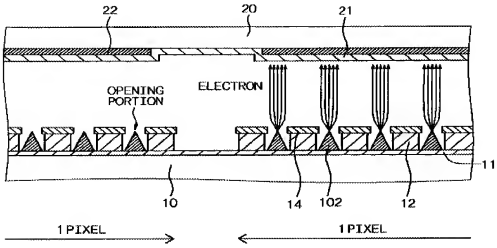
25. Kikuchi teaches a carbon area comprising carbon or a mixture with carbon as a component or a carbon compound is provided in the top, bottom, or middle of the island areas (e.g., col 18, lines 34 and 41; "the material for forming the electrode layer [i.e., the electron emitting region] includes…diamond; [and] carbon").

26. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a carbon or carbon containing compound as an electron emitting element, because carbon produces the well known effect of efficiently emitting electrons.

27. Regarding claims 24-27, Brune teaches the invention as explained above regarding claim 1, but fails to teach a transparent upper substrate and a fluorescent layer.

28. Regarding claim 24, Kikuchi teaches an imaging element (e.g., col 1, lines 17-18; "various flat panel type displays for an image displaying unit") comprising: the invention as explained above regarding claim 1 (as taught by Brune); a photoelectric conversion film approximately parallel to and opposed to the upper electrode and enclosing a vacuum space; an optically transparent electrically conducting film deposited on the photoelectric conversion film; and an optically transparent front substrate that supports the photoelectric conversion film and the optically transparent electrically conducting film (e.g., col 1, lines 52-55; "a second electrode layer (anode electrode layer) 21 [i.e., optically transparent electrically conducting film] formed on a transparent substrate 20 [i.e., optically transparent front substrate] to collide with a fluorescent layer (light emitting layer) 22 [i.e., a photoelectric conversion film] formed between the anode electrode layer 21 and the transparent substrate 20"; see Figure 33 below).

Fig. 33 (PRIOR ART)



29. Regarding claim 25, Kikuchi teaches the invention as explained above regarding claim 25 and further teaches a mesh electrode arranged within the vacuum so as to not contact the electron emitting device of the photoelectric conversion film (e.g., Figure 33 above, gate electrode 14 is a mesh electrode within the vacuum that does not contact the electron emitting element 12).

30. Regarding claim 26, Kikuchi teaches a display device comprising: the invention as explained above regarding claim 1; and an optically transparent front substrate in opposition to the upper electrode (e.g., Figure 33 above, transparent substrate 20) and enclosing a vacuum space, with a fluorescent layer arranged on the surface on the side of the vacuum space (e.g., Figure 33 above, fluorescent layer 22), and a collector electrode formed on the fluorescent layer and in opposition to the upper electrode (e.g., Figure 33 above, collector electrode 21 is formed on fluorescent layer 22 and opposite upper electrode 14).

31. Regarding claim 27, Kikuchi teaches the invention as explained above regarding claim 26 and further teaches an image display array comprising a plurality of light emitters corresponding

to the fluorescent layer (e.g., col 1, lines 25-26; "field emission display has a plurality of pixels [i.e., light emitting elements]").

32. Regarding claims 24-27, it would have been obvious to one of ordinary skill in the art at the time the invention was made to add a fluorescent layer and an anode to an electron emitting device as taught by Kikuchi, because the fluorescent layer and anode produce the well known effect of creating an image which can be used in flat panel displays.

33. Claims **17-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi in view of Sato, USPN 6,291,284 B1, published September 18, 2001 (hereinafter referred to as "Sato").

34. Regarding claim 17, Kikuchi teaches a method of manufacturing an electron emitting device (e.g., col 25, lines 17-18; "the processes for the production of the field emission device of Example 1") having a lower electrode near a substrate (e.g., col 25, lines 24-26; "the patterned electrode layer (cathode electrode layer) 11...is formed on the dielectric supporting substrate 10 constituted of a glass substrate") and an upper electrode far from the substrate respectively (e.g., col 25, lines 38-39; "a first conductive layer 14A [i.e., the layer from which upper electrode is formed by etching] composed of aluminum is formed on the insulating interlayer 12"), formed of a plurality of electron emitting elements which emit electrons from a side of the upper electrode, with space being formed between the electron emitting elements (e.g., col 26, lines 44-48; "emitter electrode 18 [i.e., electron emitting element]...can be formed in the opening portion 13A formed in the insulating interlayer 12"), and the upper electrode being extending across the plurality of electron emitting elements and the space by a bridging portion of the upper electrode (e.g., col 25, lines 43-45; "a plurality of the patterned first conductive layers 14A constituting the

gate electrodes 14 [i.e., upper electrodes] have the form of a stripe extending in a column direction [i.e., bridge portion]"), the method characterized by comprising: an electron emitting section forming step of forming a laminated body on which an upper electrode material layer is deposited to form a plurality of electron emitting elements on a substrate (e.g., col 25, lines 38-43; "a first conductive layer 14A…is formed on the insulating interlayer 12 by a sputtering method, and then the first conductive layer…14A is patterned by a known method to form the gate electrodes 14"); a bridge forming step of forming a plurality of bridge portions provided with at least one through hole or notch along a line that separates the plurality of electron emitting elements by etching the upper electrode material layer (e.g., col 25, lines 49-52; "the resist layer 40 is used as an etching mask, an opening portion 15 is formed in the gate electrode 14 by a reactive ion etching method…using chlorine base etching gas"); a cutting step of etching part of the exposed insulator layer, and either etching the substrate and lower electrode, or in subsequently carried out isotropic etching, etching the substrate and the lower electrode as far as the part that can be exposed, using the bridge portions as a mask (e.g., col 25, lines 58-62; "after the etching of the gate electrode 14 [i.e., upper electrode], while the resist layer 40 is used as an etching mask, the opening portion 13 is formed in the insulating interlayer 12 below the opening portion 15 formed in the gate electrode 14 so as to reach the electrode layer 11 [i.e., lower electrode] by an RIE method suing carbon tetrafluoride (CF_4) gas"); and a separating step of separating the exposed part of the insulator layer into the plurality of electron emitting elements by etching by isotropic etching to enlarge the space using the bridge portions as a mask (e.g., col 25, lines 63-67; "the cross section of the opening portion 13, taken by cutting the opening portion 13 with a plane perpendicular to the axial line passing through the center of the opening portion

13 and being in agreement with the axial line L passing through the center of the opening portion 15, also has a circular form having a diameter of 2 μm").

35. Kikuchi fails to teach anisotropic etching.

36. Sato teaches anisotropic etching (e.g., col 7, lines 47-51; "the patterned photoresist 6 is then used as an etching mask to etch the polycrystalline film 5' by anisotropic etching using sulfur hexafluoride (SF_6), chlorine (Cl_2) and difluoromethane (CH_2F_2) as etching gas to pattern it").

37. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use anisotropic etching as taught by Sato, in the formation of the insulation layer, because anisotropic etching has the well known characteristic of variable etch rates in different directions, leading to the benefit of controlled thickness variation in the insulation layer.

38. Regarding claim 18, Kikuchi and Sato teach the invention as explained above regarding claim 17, and Sato further teaches in the cutting step mixed gas comprising CH_2F_2, SF_6, Cl_2 is brought into contact with the exposed part of the insulator layer (e.g., col 7, lines 47-51; "the patterned photoresist 6 is then used as an etching mask to etch the polycrystalline film 5' by anisotropic etching using sulfur hexafluoride (SF_6), chlorine (Cl_2) and difluoromethane (CH_2F_2) as etching gas to pattern it").

39. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use anisotropic etching as taught by Sato, in the formation of the insulation layer, because anisotropic etching has the well known characteristic of variable etch rates in different directions, leading to the benefit of controlled thickness variation in the insulation layer.

40. Regarding claim 19, Kikuchi and Sato teach the inventions as explained above regarding claim 17 or 18, and Kikuchi further teaches in the separating step mixed gas comprising CF_4 is brought into contact with the exposed part of the insulator layer (e.g., col 25, lines 58-62; "after the etching of the gate electrode 14 [i.e., upper electrode], while the resist layer 40 is used as an etching mask, the opening portion 13 is formed in the insulating interlayer 12 below the opening portion 15 formed in the gate electrode 14 so as to reach the electrode layer 11 [i.e., lower electrode] by an RIE method suing carbon tetrafluoride (CF_4) gas").

41. Regarding claim 20, Kikuchi and Sato teach the invention as explained above regarding claim 17, and Kikuchi further teaches the electron emitting section forming step comprises: an electron supply layer forming step of forming an electron supply layer comprising silicon or a mixture whose main component is silicon or a silicon compound on the substrate (e.g., col 45, lines 18-25; "electrical conductive material may be filled in the bottom portion of the opening [i.e., the opening in the insulating interlayer]...the above electrically conductive material my be...for example, polycrystalline silicon containing an impurity"); a mask forming step of forming a mask that forms a canopy around the portion in contact with the electron supply layer on the electron supply layer (e.g., col 25, lines 58-59; "the resist layer 40 is used as an etching mask"); an insulator layer forming step of forming an insulator layer formed from a thin film of insulation material by depositing insulation material on the electron supply layer and the mask, so that around the part in contact with the mask the film thickness of the insulator layer gradually decreases to form at least one island area (e.g., col 25, lines 58-62; "the resist layer 40 is used as an etching mask, the opening portion 13 is formed in the insulating interlayer 12 below the opening portion 15 formed in the gate electrode 14 so as to reach the electrode layer 11 [i.e., so

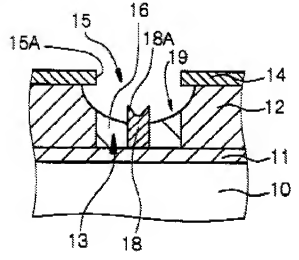
as to gradually decrease the thickness of the insulator layer to create islands]"); and an upper electrode forming step of forming a film of the upper electrode on the insulator layer to form the island area as an electron emitting section (e.g., col 25, lines 49-52; "the resist layer 40 is used as an etching mask, an opening portion 15 is formed in the gate electrode 14 by a reactive ion etching method…using chlorine base etching gas").

42. Regarding claim 21, Kikuchi and Sato teach the invention as explained above regarding claim 20, and Kikuchi further teaches a carbon area forming step of forming a carbon area comprising carbon or a mixture with carbon as a component or a carbon compound in the top, bottom, or middle of the island areas (e.g., col 18, lines 34 and 41; "the material for forming the electrode layer [i.e., the electron emitting region] includes…diamond; [and] carbon").

43. Regarding claim 22, Kikuchi and Sato teach the inventions as explained above regarding claim 20 or 21, and Kikuchi further teaches in the bridge forming step the upper electrode and the insulator layer are etched by the isotropic etching method to form bridge portions including the material part of the insulator layer integral with the insulator layers and upper electrodes of adjacent electron emitting elements, in the through holes or notches bridge portions are formed including the material part of the insulator layer, and a canopy-shaped structure made from the material of the insulator layer is formed in the through holes or notches projecting towards the center of the through holes or the inside of the notches (e.g., col 25, lines 58-62; "after the etching of the gate electrode 14 [i.e., upper electrode], while the resist layer 40 is used as an etching mask, the opening portion 13 is formed in the insulating interlayer 12 below the opening portion 15 formed in the gate electrode 14 so as to reach the electrode layer 11 [i.e., lower electrode] by an RIE method suing carbon tetrafluoride (CF_4) gas"; see also Figure 1A below,

insulator layer 12 projects in toward the center of the through hole 15 and a canopy shaped structure is produced).

Fig. 1A



44. Regarding claim 23, Kikuchi and Sato teach the invention as explained above regarding claim 20, and Kikuchi further teaches the masks are micro masks comprising a support portion that project in a direction normal to the substrate and a main mask that projects in a direction parallel to the substrate from the support portion (Note: a mask layer with any thickness other than zero, i.e., all masks, have a projection normal to the substrate as well as a projection parallel to the substrate), and the mask forming step comprises the steps of: forming a support portion material layer and a main mask material layer on the substrate; forming a resist mask thereon by photolithography so that at least part of the electron supply layer is exposed; and etching the main mask and the support portion in that order by the dry etching method and the wet etching method to form the micro masks (e.g., cols 1 and 2, lines 66-67 and 1-8; "a niobium layer is formed on a dielectric supporting substrate 10 constituted, for example, of a glass substrate, and

then the niobium layer is patterned to form an electrode layer 11. Then, an insulating interlayer 12, for example, of SiO_2 is formed on the entire surface by a CVD method. Further, a gate electrode 14 is formed, for example, by forming a metal layer on the insulating interlayer 12 by a CVD method and then patterning the metal layer. Then, an opening portion 15 is formed in the gate electrode 14 by lithography and dry etching methods. Further, the insulating interlayer 12 below the opening portion 15 is etched to form an opening portion 13 in the insulating interlayer 12").

Conclusion

45. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MARY ELLEN BOWMAN whose telephone number is (571)270-5383. The examiner can normally be reached on Monday-Thursday, 6:30 a.m.-5:00 p.m. EST.

46. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly D. Nguyen can be reached on (571) 272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

47. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. B./
Examiner, Art Unit 4174

/Jacob Y Choi/
Examiner, Art Unit 2885